I claim:

1. A microprocessor having a plurality of components which are selected from registers, arithmetic logic units, memory, input/output circuits and other similar components commonly found in microprocessors, whereby said plurality of components are interconnected in a manner which allows connection between some of the components to be varied under program control.
2. The microprocessor as claimed in claim 1, wherein said plurality of components are interconnected on a grid whereby each of said plurality of components can be switched under program control to be connected to a predetermined selection of one or more of said plurality of components.
3. The microprocessor as claimed in claim 2, further including a grid connector which provides logic for interconnecting a predetermined one or more of said plurality of components with one or more components of said plurality of components on said grid.
4. The microprocessor as claimed in claim 1, wherein said plurality of components are interconnected on a grid whereby each of said plurality of components can be switched under program control to be connected to a predetermined selection of one or more of said plurality of components, an instruction set decoder for interpreting the instruction set of said microprocessor into timed signals to said components, a clock for timing operations of said microprocessor and a grid connector which provides logic for interconnecting a predetermined one or more of said plurality of components with one or more components of said plurality of components on said grid.
5. The microprocessor as claimed in claim 2, further including at least one further grid of a plurality of further components which are selected from registers, arithmetic logic units, memory, input/output circuits and other similar components commonly found in microprocessors, said at least one further grid of a plurality of further components whereby at least a part of said grid is coupled to at least a part of said at least one further grid.